

Claim(s)

1. A multilayer chip carrier, comprising:
 - a layer of dielectric material having a plurality of signal pads formed thereon in a pattern of signal pads related to a pattern of signal pads within the footprint of at least one chip to be carried on said chip carrier, said plurality of signal pads including a first set of signal pads near the edge of said chip footprint each having a conductive line connected thereto extending beyond the edge of said chip footprint and a second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint.
2. The multilayer chip carrier as set forth in Claim 1 wherein at least some of said signal pads on said dielectric layer nearer the said edge of said chip footprint have a conductive via connected thereto that form a set of conductive vias that extend through said layer of dielectric material to the opposing surface thereof.
3. The multilayer chip carrier as set forth in Claim 2 including a further layer of dielectric material beneath said layer of dielectric material having signal pads thereon with respective ones of said signal pads connected to respective ones of said conductive vias of said set of conductive vias.

4. The multilayer chip carrier as set forth in Claim 3 wherein at least some of said signal pads on said further layer of dielectric material each have a conductive line connected thereto extending to connect to respective further signal pads nearer the edge of said chip footprint.
5. The multilayer chip carrier as set forth in Claim 4 wherein at least some of said further signal pads have conductive vias connected thereto that extend through said further layer of dielectric material to connect to signal pads on another layer of dielectric material with said signal pads on said another layer of dielectric material having conductive lines connected thereto extending beyond the edge of said chip footprint.
6. The multilayer chip carrier as set forth in Claim 5 wherein said plurality of signal pads are arranged adjacent a plurality of power distribution busses.
7. The multilayer chip carrier as set forth in Claim 6 wherein power PTHs are connected to said power distribution busses in the region of said signal pads.
8. The multilayer chip carrier as set forth in Claim 1 including a chip attached thereto.
9. The multilayer chip carrier as set forth in Claim 8 wherein said multilayer chip carrier is electrically attached to a printed wiring board.

10. A multilayer chip carrier substrate, comprising:
one layer of dielectric material having positioned thereon a plurality of
signal pads some of which form a first set of signal pads having conductive
lines connected thereto extending beyond the edge of the footprint of the chip
5 to be attached thereto and some of which form a second set of signal pads
having conductive lines connected thereto extending toward the edge of said
footprint to connect to a third set of signal pads, said third set of signal pads
having conductive vias connected thereto which are respectively connected to
a corresponding set of said signal pads on another layer of dielectric material.

10 11. The multilayer chip carrier substrate set forth in Claim 10 wherein at
least some of said signal pads of said corresponding set of signal pads on said
another layer of dielectric material have conductive lines connected thereto that
extend toward the edge of said footprint to respectively connect to a fourth set
of signal pads.

15 12. The multilayer chip carrier substrate as set forth in Claim 11 wherein at
least some of said signal pads of said fourth set of signal pads on said another
layer are connected to conductive vias which vias connect to a corresponding
set of signal pads on a further layer of dielectric material.

20 13. The multilayer chip carrier as set forth in Claim 12 wherein at least some
of said signal pads of said set of signal pads on said further layer of dielectric
material have conductive lines connected thereto extending beyond the edge of
said footprint of said chip.

14. The multilayer chip carrier as set forth in Claim 10 wherein said signal pads of said plurality of signal pads are arranged adjacent a plurality of power distribution busses.
15. The multilayer chip carrier as set forth in Claim 14 wherein power PTHs are connected to said power distribution busses on said further layer of dielectric material in the region of said first, second and third sets of signal pads.
16. The multilayer chip carrier as set forth in Claim 15 wherein said first and second set of signal pads are generally arranged in columns and rows and said power distributions busses are arranged between at least some of said columns and rows of signal pads.
17. The multilayer chip carrier as set forth in Claim 10 including a chip having an array of contacts electrically connected to pads on said chip carrier by solder connections at least some of which provide signals to said plurality of signal pads.
18. The multilayer chip carrier as set forth in Claim 17 wherein said chip carrier is electrically connected to a printed wiring board.

19. A multilayer chip carrier, comprising:

a first layer of dielectric material having a plurality of signal pads formed thereon arranged in a pattern of signal pads related to signal pads within the footprint of at least one chip to be carried by said chip carrier, said plurality of signal pads including a first set signal pads near the edge of said chip footprint each having conductive lines connected thereto extending beyond the edge of said chip footprint and a second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned closer to the edge of said chip footprint with said signal pads positioned closer to the edge of said chip footprint having conductive vias connected thereto extending through said first layer of dielectric material;

10 a second layer of dielectric material having a set of signal pads arranged thereon respectively connected to said conductive vias extending through said first layer of dielectric material and having respective conductive lines connected thereto extending to respectively connect to further signal pads positioned closer to the edge of said chip footprint, said further signal pad having conductive vias connected thereto extending through said second layer of dielectric material; and

15 a third layer of dielectric material having a set of signal pads arranged thereon respectively connected to the said conductive vias extending through said second layer of dielectric material and having conductive lines respectively connected thereto extending beyond the edge of said chip footprint.

20. The multilayer chip carrier as set forth in Claim 19 including at least one chip having a pattern of electrical contacts corresponding to said pattern of signal pads electrically connected thereto.
21. The multilayer chip carrier as set forth in Claim 20 wherein said chip carrier is electrically attached to a printed wiring board.
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22. A method of fanout redistribution of signal pads on a multilayer chip carrier, comprising:
 - providing a layer of dielectric material having a plurality of signal pads formed thereon in a pattern of signal pads within the footprint of at least one chip to be carried therein;
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 - providing conductive lines connected to a first set of signal pads of said plurality of signal pads near the edge of said chip footprint extending beyond the edge of said chip footprint to allow signals from said first set of signal pads to escape said chip footprint; and
 - 15 moving a second set of signal pads of said plurality of signal pads closer to the edge the edge of said chip footprint.
23. The method as set forth in Claim 22 including the step of providing at least some of said signal pads moved closer to the edge of said chip footprint with connections to signal pads on another layer of dielectric material below said layer of dielectric material.
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24. The method as set forth in Claim 23 including the step of moving at least some of said signal pads on said another layer of dielectric material closer to the edge of said chip footprint.
25. The method as set forth in Claim 24 including the step of providing at least some of said signal pads on said another layer of dielectric material moved closer to the edge of said chip footprint with connections to signal pads on a further layer of dielectric material below said another layer of dielectric material.
26. The method as set forth in Claim 25 including the step of providing conductive lines connected to at least some of the said signal pads on said further layer of dielectric material that extend beyond the edge of said chip footprint to allow signals from said signal pads on said further layer to escape said chip footprint.
27. The method as set forth in Claim 26 wherein said plurality of signal pads are arranged adjacent a plurality of power distribution busses.
28. The method as set forth in Claim 27 wherein PTHs are connected to said power distribution busses in the region of said moved signal pads.
29. The method as set forth in Claim 28 wherein at least one chip is attached to said multilayer chip carrier.

30. The method as set forth in Claim 29 wherein said multilayer chip carrier is attached to a printed wiring board.